Refine Search

Search Results -

Terms	Documents
(712/43 |712/202 |712/203 |712/206 |712/207 |712/34).ccls.	1142

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L7

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Thursday, December 29, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L7	712/43,202,203,206,207,34.ccls.	1142	L7
L6	712/208,209,43,202,203.ccls.	897	L6
L5	710/29.ccls.	371	L5
L4	712/217,222,23.ccls.	1158	L4
L3	709/224.ccls.	2455	L3
L2	717/118.ccls.	153	L2
L1	717/136,137,138,139.ccls.	497	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(register$ near4 based) and (stack$ near5 based) and operand$ and exception$ and overflow and underflow$ and (switch$ near4 mode$)	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L11

Refine Search

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Search History

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Set Name side by side	Query	Hit Count	Set Name result set
DB=TDBD; PLUR=YES; OP=ADJ			
L11	(register$ near4 based) and (stack$ near5 based) and operand$ and exception$ and overflow and underflow$ and (switch$ near4 mode$)	0	L11
DB=DWPI; PLUR=YES; OP=ADJ			
L10	(register$ near4 based) and (stack$ near5 based) and operand$ and exception$ and overflow and underflow$ and (switch$ near4 mode$)	0	L10
DB=JPAB; PLUR=YES; OP=ADJ			
L9	(register$ near4 based) and (stack$ near5 based) and operand$ and exception$ and overflow and underflow$ and (switch$ near4 mode$)	0	L9
DB=EPAB; PLUR=YES; OP=ADJ			
L8	(register$ near4 based) and (stack$ near5 based) and operand$ and exception$ and overflow and underflow$ and (switch$ near4 mode$)	0	L8
DB=USOC; PLUR=YES; OP=ADJ			

L7	(register$ near4 based) and (stack$ near5 based) and operand$ and exception$ and overflow and underflow$ and (switch$ near4 mode$)	0	L7
DB=PGPB; PLUR=YES; OP=ADJ			
L6	(register$ near4 based) and (stack$ near5 based) and operand$ and exception$ and overflow and underflow$ and (switch$ near4 mode$)	4	L6
DB=USPT; PLUR=YES; OP=ADJ			
L5	(register$ near4 based) and (stack$ near5 based) and operand$ and exception$ and overflow and underflow$ and (switch$ near4 mode$)	2	L5
L4	L3 and accelarator$ and cpu	0	L4
L3	(register$ near4 based) and (stack$ near5 based) and operand$ and exception$ and overflow and underflow$	27	L3
L2	register-based and stack-based and operand and exception$ and overflow and underflow$	2	L2
L1	register-based and stack-based and opernd and exception$ and overflow and underflow$	0	L1

END OF SEARCH HISTORY

Terms used
processing and **cpu** and **accelerator** and **stack** and **register** and **instruction** and **overflow** and **underflow** and

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Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next
Best 200 shown Releva

1 Real-time shading
Marc Olano, Kurt Akeley, John C. Hart, Wolfgang Heidrich, Michael McCool, Jason L. Mitchell, Randi
August 2004 **Proceedings of the conference on SIGGRAPH 2004 course notes GRAPH '04**
Publisher: ACM Press
Full text available: pdf(7.39 MB) Additional Information: full citation, abstract

Real-time procedural shading was once seen as a distant dream. When the first version of this c offered four years ago, real-time shading was possible, but only with one-of-a-kind hardware or combining the effects of tens to hundreds of rendering passes. Today, almost every new compu with graphics hardware capable of interactively executing shaders of thousands to tens of thous instructions. This course has been redesigned to address today's real-time shading capabili ...

2 Design and verification of the Rollback Chip using HOP: a case study of formal methods a hardware design
Ganesh Gopalakrishnan, Richard Fujimoto
May 1993 **ACM Transactions on Computer Systems (TOCS)**, Volume 11 Issue 2
Publisher: ACM Press
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The use of formal methods in hardware design improves the quality of designs in many ways: it better understanding of the design; it permits systematic design refinement through the discov invariants; and it allows design verification (informal or formal). In this paper we illustrate the u methods in the design of a custom hardware system called the "Rollback Chip" (RBC), conducte simple hardware design description language called "HOP&r ...

3 The elements of nature: interactive and realistic techniques
Oliver Deusen, David S. Ebert, Ron Fedkiw, F. Kenton Musgrave, Przemyslaw Prusinkiewicz, Doug I Stam, Jerry Tessendorf
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Terms used
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Sort results by relevance

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Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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Results for "(((stack and register and instruction and processor and accelerator and overflow))<in>metadat..." e-mail
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Check to search only within this results set

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» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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